

FIG. 1

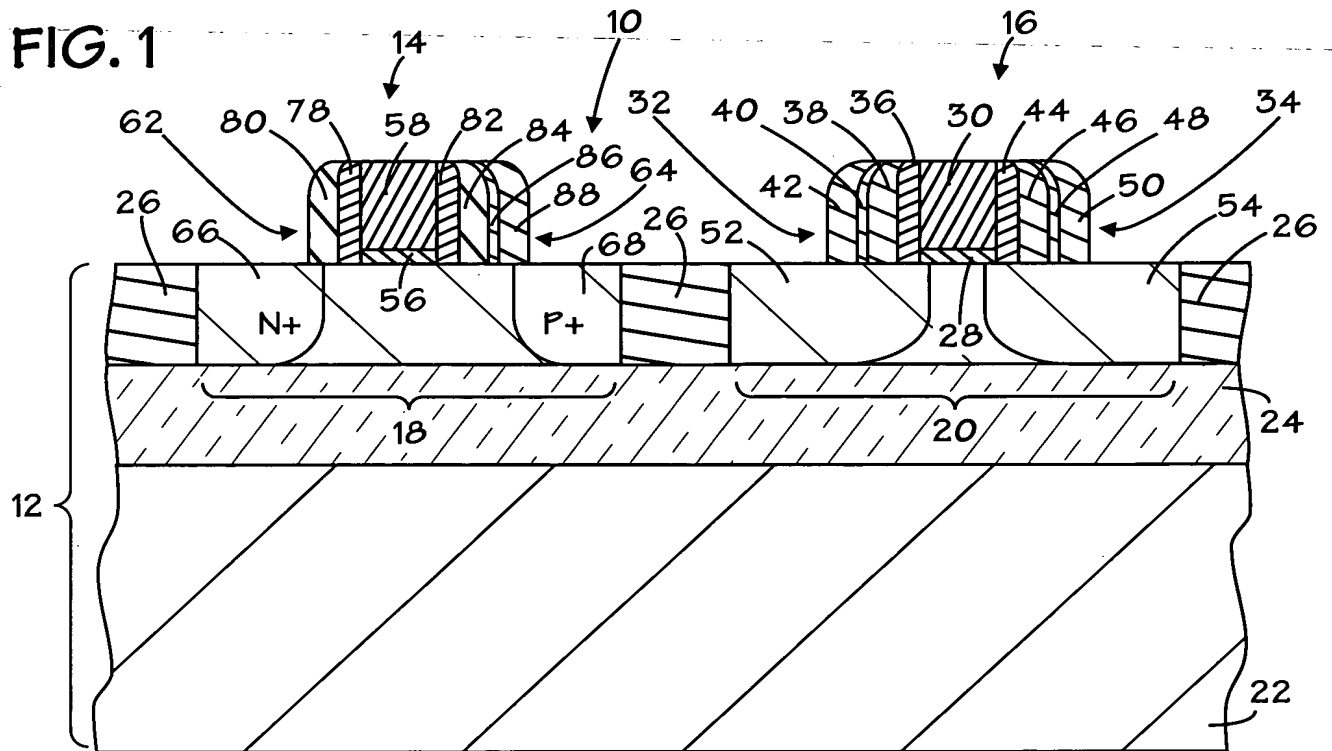
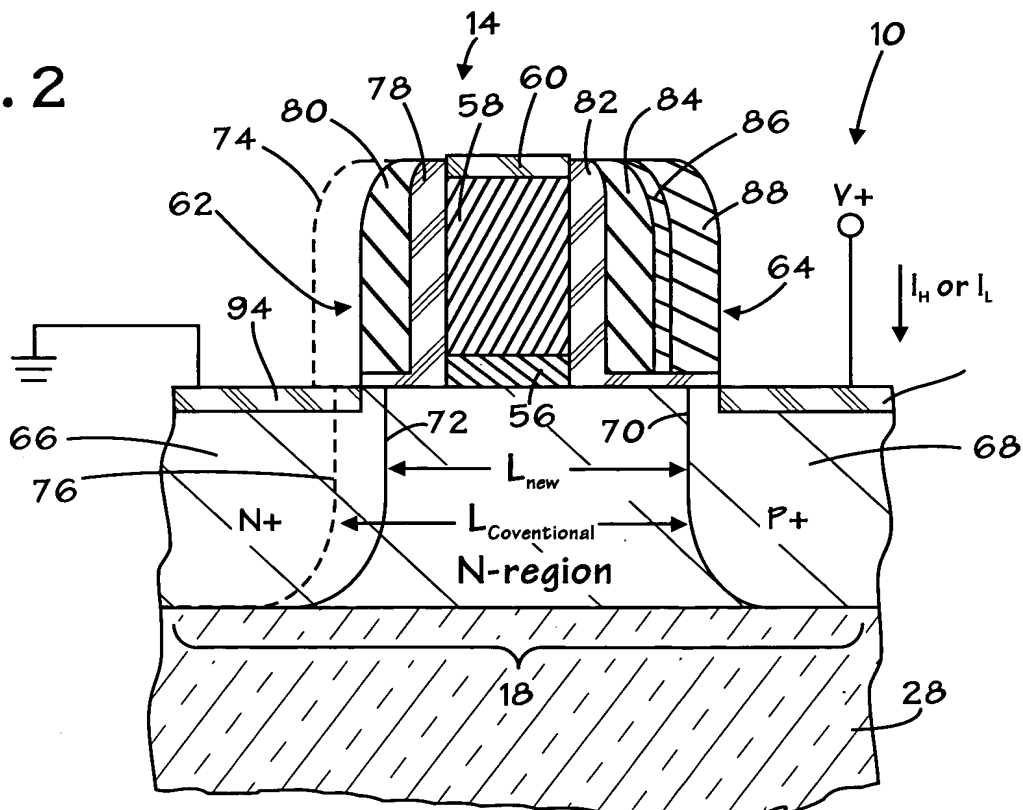


FIG. 2



A cross-sectional view of a semiconductor device. The device features a substrate with an N-region and a P+ region. A gate stack is formed on the N-region, consisting of a gate dielectric (100) and a gate electrode (102). The gate electrode is divided into segments (80, 82, 84, 86, 88) by spacers (78, 82, 84, 86, 88). The spacers are formed by a sequence of layers: a first layer (58), a second layer (82), a third layer (84), and a fourth layer (86). The first layer (58) is a conductive layer, and the subsequent layers (82, 84, 86) are insulating layers. The device is shown with a top surface (106) and a bottom surface (104). The N-region is labeled "N-region" and the P+ region is labeled "P+". The substrate is labeled "18" and "28".

A cross-sectional view of a semiconductor device. At the top, a series of downward-pointing arrows represent incident light or radiation, with a label 110 at the top right. The device consists of a substrate 12 with a bottom layer 18. Above the substrate is a layer 28. A central N-region 70 is flanked by P+ regions 72 and 74. A layer 56 is on top of the N-region. A central structure 62 is formed on top of the N-region, with a central core 82 and side regions 80 and 84. A layer 98 is on top of the central structure. A layer 86 is on top of the P+ regions. A layer 88 is on top of the N-region. A layer 108 is on top of the P+ regions. A layer 64 is on top of the N-region. A layer 10 is on top of the P+ regions. A layer 110 is on top of the P+ regions.

[illegible]